AKHIL RAJ BARANWAL

website

Design Engineer at Imagination Technologies, India
interested in Computer Architecture and Systems for ML

EDUCATION

B.E. in Electronics and Instrumentation Jul 2016 – Aug 2020
Birla Institute of Technology and Science, Pilani

WORK EXPERIENCE

- **CPU Design Engineer, Imagination Technologies** Aug 2022 – Present
  Investigation, specification, implementation, and delivery of CPU micro-architecture components.
- **ASIC Verification Engineer, Micron Technology** Aug 2020 – Aug 2022
  SoC verification of host-interface involving the UFS protocol for storage controllers. Also involved in first post-silicon bringup of new internal architecture.
- **Guest Researcher, CFAED - Technische Universität Dresden** Jan 2020 – Jun 2020
  Worked with the Chair for Processor Design, CFAED, exploring and implementing accelerator-designs for reinforced learning problems.
- **Embedded Engineering Intern** May 2019 – Jul 2019
  Worked on encrypted high speed memory-trace collection and analysis of DRAM AXI traffic in PetaLinux.
- **Engineering Intern** May 2018 – Jul 2018
  Developed a GSM interface for controlling industrial machines spread across an area of more than 1600 acres.

PUBLICATIONS

- **ReLAccS: A Multi-level Approach to Accelerator Design for Reinforcement Learning on FPGA-based Systems** [Click here]
  IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. (Volume: 40, Issue: 9, Page(s): 1754-1767) Oct 2020

- **MemOReL: A Memory-oriented Optimization Approach to Reinforcement Learning on FPGA-based Embedded Systems** [Click here]
  Proceedings of the 2021 on Great Lakes Symposium on VLSI. (Pages: 339–346) Jun 2021

- **Development of Completely Automated Poly Potential Portable Potentiostat** [Click here]
  ECS Journal of Solid State Science and Technology. (Volume: 10, Number: 2) Feb 2021

PROJECTS

- **Elliptically Compensated Spectrophotometer** Jan 2019 – Apr 2018
  Worked with the MNNE Lab to build an approximate spectrophotometer for excitation frequencies in the visible spectrum. Links:
- **Fault Tolerant Network on Chips** Aug 2018 – Dec 2018
  Worked with Dr. Soumya J to propose a new algorithm for fault-tolerant packet-routing strategy for link faults between routers that occur either during manufacturing or in-operation. Links:
- **VMS** May 2018 - July 2018
  Python utility to sync multiple devices playing the same video using MQTT which syncs timestamps instead of video frames, offering significantly less network usage. Links:

SKILLS

- C/++, Python, Verilog, Computer Architecture